REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of November 30, 2005 (hereinafter "Office Action"). Applicants especially appreciate the allowance of Claims 8 - 13. In response, Applicants respectfully submit that Claims 1 - 7 and 14 - 24 satisfy the requirements of 35 U.S.C. §112 and that the cited references do not disclose or suggest all of the recitations of independent Claims 25 and 26. Accordingly, Applicants submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Claims 1 - 7 and 14 - 24 Satisfy the Requirements of 35 U.S.C. §112

Independent Claim 1 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite. In particular, the Office Action states that the error signal recited in line 3 of Claim 1 is unclear because it is unclear what kind of error signal it is and how it is detected. The Office Action also states that it is unclear whether the error signal recited in line 7 is the same error signal that is recited in line 3. (Office Action, page 2). Applicants respectfully submit that there is no lack of clarity in the way the "error signal" recitation is used in Claim 1. There is only one "error signal" recited in Claim 1. The "error signal" recitation is first introduced in line 3 and is preceded by the indefinite article "a." Subsequently, the "error signal" recitation is preceded by the definite article "the" in lines 5 and 7 thereby indicating reference to the same "error signal" introduced in line 3. Lines 6 - 8 of Claim 1 explain that the phase detector circuit generates the error signal responsive to the first and second clock signals. Thus, Applicants submit that all elements recited in independent Claim 1 are fully cooperated as the phase detector circuit connects the first clock circuit to the second clock circuit, the error signal generated by the phase detector is an input to the first and second clock circuits, and the first and second clock signals generated by the first and second clock circuits, respectively, are inputs to the phase detector circuit.

With regard to dependent Claim 2, the analysis applied above with respect to independent Claim 1 is applicable to this claim. There is only one "second error signal"

recited in Claim 2. The " second error signal" recitation is first introduced in line 5 and is preceded by the indefinite article "a." Subsequently, the "second error signal" recitation is preceded by the definite article "the" in lines 7 and 10 thereby indicating reference to the same "second error signal" introduced in line 5. Lines 6 - 8 of Claim 1 explain that the second phase detector circuit generates the second error signal responsive to the first and third clock signals. Thus, Applicants submit that all elements recited in independent Claim 2 are fully cooperated as the second phase detector circuit connects the first clock circuit to the third clock circuit, the second error signal generated by the second phase detector is an input to the first and third clock circuits, and the first and third clock signals generated by the first and third clock circuits, respectively, are inputs to the second phase detector circuit.

With regard to Claims 14, 15, 19, and 20, Applicants submit that these claims are not indefinite for the same reasons discussed above with respect to Claims 1 and 2. In view of the foregoing, Applicants submit that Claims 1 - 7 and 14 - 24 comply with 35 U.S.C. §112 and respectfully request that the §112 objection be withdrawn.

Independent Claims 25 and 26 are Patentable

Independent Claims 25 and 26 stand rejected under 35 U.S.C. §103(a) as being obvious over U. S. Patent No. 6,516,422 to Doblar et al. (hereinafter "Doblar") in view of U. S. Patent No. 6,510,013 to Oshio (hereinafter "Oshio").

Independent Claim 25 is directed to a method of distributing a clock signal over an integrated circuit and recites, in part:

> ...
> synchronizing phases of the plurality of clock signals to one another based on error signals that are generated based on relative phase differences between ones of the plurality of clock signals.

Independent Claim 26 includes similar recitations. Thus, according to independent Claims 25 and 26, multiple clock signals are synchronized to one another based on multiple error signals that are generated based on relative phase differences between ones of the clock signals.

The Office Action acknowledges that Doblar does not disclose or suggest the

recitation of Claim 25 reproduced above, but alleges that Oshio provides the missing teaching. (Office Action, pages 3 and 4).

Doblar describes a system and method for providing redundant, synchronized clocks in a computer system (Doblar, Abstract) in which a clock board 0 105A and a clock board 1 105B are used. Doblar explains that one of the clock boards 0 and 1 (105A and 105B) is used to generate a master clock signal and the other of the clock boards 0 and 1 is used to generate a slave clock signal. If the master clock board were to fail, then the slave clock board may take over to generate the master clock signal. (Doblar, col. 3, lines 39 - 46). Referring to FIG. 2, Doblar further explains that, for example, if clock board 0 is the master board, then the output of the filter 215A, which generates a feedback signal based on a phase difference between the output clock signals of the clock boards 0 and 1, is not provided to the voltage controlled oscillator 220A. Instead, a constant voltage is used to drive the voltage controlled oscillator 220A. (Doblar, col. 4, 34 - 40). It is only when the clock board 0 is used to generate the slave clock signal that the output of the filter 215A is provided to the voltage controlled oscillator 220A to generate the output clock signal 106A. (Doblar, col. 4, lines 41 - 42; *see also*, col. 4,line 58 - col. 5, line 3).

Thus, in sharp contrast to the recitations of independent Claim 25 which states that multiple clock signals are synchronized to one another based on multiple error signals that are generated based on relative phase differences between ones of the clock signals, Doblar describes a system in which *only* the slave clock signal is generated responsive to an error signal, which is based on a phase difference between the master clock signal and the slave clock signal, but the master clock signal is not generated responsive to an error signal generated based on a relative phase difference between at least two clock signals. Rather, the master clock signal is generated responsive to a constant voltage used to drive a voltage-controlled oscillator as discussed above.

Applicants further submit that Oshio fails to provide the missing teachings. Oshio describes a phase-synchronization method and circuit in which an error signal is generated by a demodulator based on a difference between a synchronizing signal pattern and a synchronization pattern on a magnetic disk. (Oshio, col. 2, line 63 - col. 3, line 4; col. 6, lines

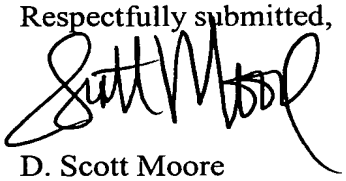
56 - 65). The error signal may be coupled to a voltage-controlled oscillator 12 via a phase error detection circuit 13 and a switch circuit 14, 15 as shown in FIGS. 3 and 6. Thus, if the teachings of Oshio were to be combined with Doblar, then the phase error detection circuit 13 and switch circuit 14, 15 of Oshio may be used in place of the switch circuits 218A and 218B shown in FIG. 2 of Doblar. Similar to the switches 218A and 218B of Doblar, switches 14 and 15 of Oshio are used to drive a voltage-controlled oscillator with either an error signal or a fixed voltage, e.g., a zero voltage. (Oshio, FIGS. 3, 6 and 7; col. 3, lines 23 - 55; col. 6, line 66 - col. 7, line 56). As a result, the combination of Doblar with Oshio would still not result in the master clock signal of Doblar being generated responsive to an error signal that is based on a relative phase difference between at least two clock signals. Even if Doblar were to be modified with the teachings of Oshio, the master clock signal would be generated responsive to a constant voltage or ground potential used to drive a voltage-controlled oscillator as discussed above.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 25 and 26 are patentable over the cited references.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



D. Scott Moore
Registration No. 42,011

Customer No. 20792
Myers Bigel Sibley & Sajovec
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401

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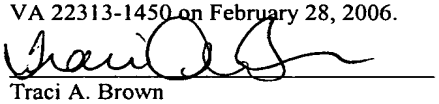

Traci A. Brown